

IN THE CLAIMS

Please amend the Claims as shown below:

Please cancel Claim 14 without prejudice.

Please amend the Claims as shown below:

Sub C1
15. (Amended) The process of Claim 16, comprising forming an oxide over said silicided bitline.

16. (Amended) A process of fabricating a memory cell comprising a substrate that comprises a first region and a second region with a channel therebetween, the method comprising:

forming a gate above said channel of said substrate, wherein said gate comprises a polysilicon layer;

forming a bitline; and

siliciding said bitline.

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Con't Sub C1
19. (Amended) The process of Claim 16, comprising:
forming a charge trapping region that contains a first amount of charge; and

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COND

forming a layer between said channel and said charge trapping region, wherein said layer has a thickness such that said first amount of charge is prevented from directly tunneling into said layer.

003 Sub
C1

21. (Amended) The process of Claim 16, wherein said gate comprises an N-type material.

Sub
C1

26. (Amended) The process of Claim 16, wherein said memory cell comprises an EEPROM memory cell.

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27. (Amended) The process of Claim 16, wherein said memory cell comprises a two-bit memory cell.

28. (Amended) The process of Claim 16, wherein said substrate comprises a P-type substrate.

29. (Amended) The process of Claim 16, further comprising scaling the length of said bitline.